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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,732	02/27/2004	Chenghung Justin Chen	200400184-1	8404

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EXAMINER	
FAHERTY, COREY S	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
02/01/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/789,732	CHEN ET AL.	
	Examiner	Art Unit	
	Corey S. Faherty.	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/26/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-16 and 18-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-16 and 18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the reply filed on 12/26/2007.

2. Claims 1-5, 7-16 and 18-29 are pending in the application and have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-16 and 18-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson et al. (*Cyclical Cascade Chains: A Dynamic Barrier Synchronization Mechanism for Multiprocessor Systems*), referenced from here forward as Johnson.

5. Regarding claims 1 and 12, Johnson discloses a method of synchronizing a plurality of processors of a multi-processor computer system on a synchronization point [page 1, abstract], comprising:

triggering a first set of processors to enter an entry holding loop in response to said first set of processors encountering said synchronization point before a lead processor associated with said plurality of processors [page 5, first column, paragraph 2; Figure 6; when a processor reaches a barrier, it sends a pulse to the left-most flip-flop, causing the flip-flop to be set; the processor is then in an "entry holding loop" while it waits for other processors to reach the barrier];

triggering said first set of processors to enter an exit holding loop in response to said lead processor encountering said synchronization point [page 5, first column, paragraph 2; Figure 6; the last processor to reach the barrier constitutes the lead processor; when this lead processor reaches the barrier, the signals output from the left-most flip-flops propagate to the outputs, indicating that each processor is synchronized];

triggering said plurality of processors to leave said exit holding loop in response to a tail processor associated with said plurality of processors encountering said synchronization point [page 5, first column, paragraph 2; Figure 6; when the propagation of output signals reaches the last processor, all of the processors are synchronized, the left-most flip-flops are reset, and the processors resume execution synchronously]; and

wherein the triggering occurs without accessing a shared memory area of said multi-processor system [section 5].

6. Regarding claims 2, 13 and 23, Johnson discloses the method of claim 1 further comprising creating a circular reference arrangement for said plurality of processors [page 4, first column, second paragraph; the processors are arranged as a cyclical doubly linked list], wherein a first processor from among said plurality of processors is designated said lead processor and a second processor from among said plurality of processors is designated said tail processor, and wherein said lead processor is adjacent to said tail processor in said circular reference arrangement [page 5, first column, paragraph 2; Figure 6; the last processor to reach the barrier constitutes the lead processor; the processor that is above the lead processor is the tail processor; page 6, section 6; alternatively, the lead processor is that which calls the wait routine].

7. Regarding claims 3, 14 and 24, Johnson discloses the method of claim 2 wherein said circular reference arrangement represents a circular linked list [page 4, first column, second paragraph; the processors are arranged as a cyclical doubly linked list].

8. Regarding claims 4 and 15, Johnson discloses the method of claim 2 wherein said triggering said first set of processors is performed in a cascading manner starting with said lead processor following a sequence established by said circular reference arrangement, with each processor of said first set of processors being triggered by its immediate predecessor in said sequence [section 5; Figure 6; the processors are connected in a circular fashion so that each indicates to another when it is ready to proceed beyond the barrier].

9. Regarding claims 5 and 16, Johnson discloses the method of claim 4 wherein said triggering said plurality of processors is performed in a cascading manner starting with said tail processor following said sequence established by said circular reference arrangement, with each processor of said plurality of processors being triggered by its immediate predecessor in said sequence [section 5; Figure 6; the processors are connected in a circular fashion so that each indicates to another in a cascading manner when it has completed synchronization].

10. Regarding claims 7, 18 and 25, Johnson discloses the method of claim 6 wherein said triggering said first set of processors employs a first external interrupt mechanism associated with each of said first set of processors [page 6, first column, second full paragraph; the signals used to indicate that a processor has reached a barrier are externally input].

11. Regarding claims 8, 19 and 26, Johnson discloses the method of claim 7 wherein said triggering said first set of processors includes writing to hard physical addresses of each of said

first set of processors [page 6, first column, last paragraph, second column, first full paragraph; a processor may specifiy the processor in which it will write its *SendTo* signal].

12. Regarding claims 9, 20 and 27, Johnson discloses the method of claim 6 wherein said triggering said plurality of processors employs a second external interrupt mechanism associated with each of said plurality of processors [page 6, first column, second full paragraph; the signals used to indicate that a processor has reached a barrier are externally output].

13. Regarding claims 10, 21 and 28, Johnson discloses the method of claim 9 wherein said triggering said plurality of processors includes writing to hard physical addresses of each of said plurality of processors [page 6, first column, last paragraph, second column, first full paragraph; a processor may specify the processor in which it will write its *SendTo* signal].

14. Regarding claims 11, 22 and 29, Johnson discloses the method of claim 1 wherein said triggering said first set of processors employs a masked interrupt approach [page 6, section 6; a masking technique is used to determine which processors will be interrupted by the barrier].

Response to Arguments

15. Applicant's arguments filed 12/26/2007 have been fully considered but they are not persuasive. In general, applicant disagrees with the examiner's position that the teachings of Johnson anticipate the invention of the claims. However, to support this position, applicant has offered no specific arguments or evidence but instead makes vague statements that certain teachings of Johnson do not teach certain portions of the claims. It is therefore difficult for the examiner to even determine what portions of the claim applicant believes are not taught by Johnson. Still, the examiner has reviewed these stated positions and respectfully disagrees with

them. Judging from the emphasis placed in the claim language of page 14 of the reply, it appears that applicant believes Johnson does not teach the claimed "entry holding loop" and "exit holding loop". Though it is not clear on what basis applicant has taken this position, the examiner respectfully disagrees on the basis that these terms are broad and have not been sufficiently defined in the present claim language in order to distinguish over Johnson. As they are currently claimed, the "entry holding loop" and "exit holding loop" are no more than simple states that a processor may be in. The examiner therefore respectfully suggests that, in order to overcome the Johnson reference, further detail regarding the nature of the "entry holding loop" and "exit holding loop" be explicitly recited in the claims.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Corey S Faherty
Examiner
Art Unit 2183

CF

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